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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,773	10/24/2003	Heon Lee	200316030-1	8956

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EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,773	LEE, HEON	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *21-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102 or 103

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 5-9, 11 and 15-19 stand rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Costrini (U.S. Patent Appl. Pub. No. 2004/0063223).

4. As to claim 1, Costrini discloses a method of making a magnetic tunnel junction device, comprising: forming a magnetic tunnel junction stack (100) (paragraph 0011; Figure 2B); forming an etch stop layer (125) on the magnetic tunnel junction stack (100) (Figure 2B), the etch stop layer comprising a first electrically conductive material (paragraph 0011); forming a single layer of first mask layer (60) (paragraph 0017, "[a]lternative hardmask materials, such as TiN or TaN..."; Figure 3) on the etch stop

layer (125) (paragraph 0011; Figure 3); patterning the first mask layer (60) (paragraph 0017; Figure 3); forming a discrete magnetic tunnel junction stack by etching the magnetic tunnel junction stack (paragraph 0017; Figure 3); forming a spacer layer (72) on the discrete magnetic tunnel junction stack, the spacer layer comprising an electrically non-conductive material (paragraph 0020; Figure 4); forming a spacer (82) by anisotropically etching the spacer layer (72) (paragraph 0020; Figure 5); forming a dielectric layer (86) over the discrete magnetic tunnel junction stack and the spacer (82) (paragraph 0023; Figure 6); planarizing the dielectric layer (86) to form a substantially planar surface that is co-planar with an the exposed portion of the first mask layer (60) (paragraph 0023;Figures 5-6); forming a self-aligned via (66) by etching away the first mask layer (60) (paragraph 0023; Figure 6); and depositing a second electrically conductive material (92/95) on the dielectric layer (86) and in the self-aligned via (66) (paragraph 0023; Figure 7).

5. Although Costrini does not expressly disclose patterning the second electrically conductive material and forming a dual-damascene conductor by etching the second electrically conductive material, these steps are an inherently present in forming the device. *See* Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002) ("Wolf II"), pages 671-72, Figure 15-1. In the alternative, Applicant's claimed steps of patterning the second electrically conductive material and forming a dual-damascene conductor by etching the second electrically conductive material, would have obvious to one of ordinary skill in the art at the time the invention was made, because Wolf II

teaches these steps are commonly used in forming the final device structure (pages 671-72, Figure 15-1).

6. As to claim 5, Costrini discloses that the depositing of the second electrically conductive material (92/95) is continued until the second electrically conductive material completely fills the self-aligned via (66) and extends outward of the substantially planar surface by a predetermined distance (paragraphs 0023, 0025; Figure 8).

7. As to claim 6, Costrini discloses that the etching the first mask layer is continued until the first mask layer is completely dissolved and the self-aligned via extends to the etch stop layer (paragraph 0023; Figure 6). Etch stop layer (125) caps layer (120/122) (paragraph 0011).

8. As to claim 7, Costrini discloses that the spacer layer (72) is conformally deposited on the discrete magnetic tunnel junction stack (paragraph 0020; Figure 4).

9. As to claim 8, Costrini discloses that the spacer layer (72) comprises a material selected from the group consisting of silicon oxide and silicon nitride (paragraph 0020).

10. As to claim 9, Costrini discloses that the anisotropically etching the spacer layer (72) comprises a reactive ion etch (paragraphs 0020; 0004).

11. As to claim 11, Costrini discloses a method of making a magnetic tunnel junction device from a previously fabricated magnetic tunnel junction stack (paragraph 0011; Figure 2B), comprising: forming an etch stop layer (125) on the magnetic tunnel junction stack (100) (Figure 2B), the etch stop layer comprising a first electrically conductive material (paragraph 0011); forming a single layer of first mask layer (60) (paragraph 0017, "[a]lternative hardmask materials, such as TiN or TaN..."; Figure 3) on

the etch stop layer (125) (paragraph 0011; Figure 3); patterning the first mask layer (60) (paragraph 0017; Figure 3); forming a discrete magnetic tunnel junction stack by etching the magnetic tunnel junction stack (paragraph 0017; Figure 3); forming a spacer layer (72) on the discrete magnetic tunnel junction stack, the spacer layer comprising an electrically non-conductive material (paragraph 0020; Figure 4); forming a spacer (82) by anisotropically etching the spacer layer (72) (paragraph 0020; Figure 5); forming a dielectric layer (86) over the discrete magnetic tunnel junction stack and the spacer (82) (paragraph 0023; Figure 6); planarizing the dielectric layer (86) to form a substantially planar surface that is co-planar with an the exposed portion of the first mask layer (60) (paragraph 0023;Figures 5-6); forming a self-aligned via (66) by etching away the first mask layer (60) (paragraph 0023; Figure 6); and depositing a second electrically conductive material (92/95) on the dielectric layer (86) and in the self-aligned via (66) (paragraph 0023; Figure 7).

12. Although Costrini does not expressly disclose patterning the second electrically conductive material and forming a dual-damascene conductor by etching the second electrically conductive material, these steps are an inherently present in forming the device. *See* Wolf II, pages 671-72, Figure 15-1. In the alternative, Applicant's claimed steps of patterning the second electrically conductive material and forming a dual-damascene conductor by etching the second electrically conductive material, would have obvious to one of ordinary skill in the art at the time the invention was made, because Wolf II teaches these steps are commonly used in forming the final device structure (pages 671-72, Figure 15-1).

13. As to claim 15, Costrini discloses that the depositing of the second electrically conductive material (92/95) is continued until the second electrically conductive material completely fills the self-aligned via (66) and the first electrically conductive material (92/95) extends outward of the substantially planar surface by a predetermined distance (paragraphs 0023, 0025; Figure 8).

14. As to claim 16, Costrini discloses that the etching the first mask layer is continued until the first mask layer is completely dissolved and the self-aligned via extends to the etch stop layer (125) (paragraph 0023; Figure 6). Etch stop layer (125) caps layer (120/122) (paragraph 0011).

15. As to claim 17, Costrini discloses that the spacer layer (72) is conformally deposited on the discrete magnetic tunnel junction stack (paragraph 0020; Figure 4).

16. As to claim 18, Costrini discloses that the spacer layer (72) comprises a material selected from the group consisting of silicon oxide and silicon nitride (paragraph 0020).

17. As to claim 19, Costrini discloses that the anisotropically etching the spacer layer (72) comprises a reactive ion etch (paragraphs 0020; 0004).

Claim Rejections - 35 USC § 103

18. Claims 2-4 and 12-14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Costrini, in view of Wolf et al., *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (1986) ("Wolf I").

19. As to claims 2 and 12, Costrini does not expressly disclose that the etching away the first mask layer comprises a plasma etch using an etch material comprising a gas

containing fluorine. However, Costrini discloses that first mask layer (60) is formed of nitride (62) and oxide (64) (paragraph 0017; Figure 3). Wolf I teaches that for gas etching nitrides and oxides, a gas containing fluorine is conventional (page 581). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to etch away the first mask layer comprises a plasma etch using an etch material comprising a gas containing fluorine. One who is skilled in the art would be motivated to use a conventional gas for etching oxides and nitrides, because such gases are known to accomplish dry etching.

20. As to claims 3 and 13, Costrini does not expressly disclose that the etch material further includes oxygen. However, Costrini discloses that first mask layer (60) is formed of nitride (62) and oxide (64) (paragraph 0017; Figure 3). Wolf I teaches that for gas etching nitrides, a gas containing fluorine and oxygen is conventional (page 581). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an etch material further including oxygen. One who is skilled in the art would be motivated to use a conventional gas for etching nitrides, because such gases are known to accomplish dry etching.

21. As to claims 4 and 14, Costrini does not expressly disclose that the etching of the first mask layer to form the self-aligned via comprises a wet etch using an etchant material including fluorine. However, Costrini discloses plasma etching to form the self-aligned via (66) (paragraph 0023). Moreover, Costrini discloses that first mask layer (60) is formed of nitride (62) and oxide (64) (paragraph 0017; Figure 3). Wolf I teaches that the advantages of wet etching include low cost, reliability, high throughput process

with excellent selectivity (page 529). Moreover, etchant materials including fluorine, such as HF solutions, are commonly used to etch oxides (pages 532-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to a wet etch using an etchant material including fluorine. One who is skilled in the art would wet etch for its known benefits and to use a conventional solution, known to accomplishing etching.

Claim Rejections - 35 USC § 103

22. Claims 10 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Costrini, in view of Chen (U.S. Patent No. 6,627,913).

23. As to claims 10 and 20, Costrini does not expressly disclose that after the forming of the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other. However, Chen discloses a discrete magnetic tunnel junction stack (10) (column 4, lines 14-18; Figure 3) with spacers (50) (column 5, lines 6-7; Figure 5). Chen teaches that the spacers (50) function to alleviate problems with mask misalignment (column 5, lines 49-50), such as overetching along the side of the magnetic tunnel junction stack (column 2, lines 25-30; Figure 2). Moreover, Chen teaches that with the presence of spacer (50) results in greater design tolerances in mask alignment (column 6, lines 14-17, lines 22-24; Figure 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the self-aligned via, the discrete magnetic tunnel junction stack and

the self-aligned via are not aligned relative to each other. One who is skilled in the art would be motivated to adopt a process with greater design tolerances.

Terminal Disclaimer

24. The Terminal Disclaimer filed on Sept. 28, 2005, disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of Lee (U.S. Patent Appl. Pub. No. 2005/0090056) or Lee (U.S. Patent Appl. Pub. No. 2005/0090119) has been reviewed and is accepted. The Terminal Disclaimer has been recorded.

Response to Arguments

25. In view of Applicant's claim amendments (Applicant's Listing of the Claims, claims 1 and 11), filed Sept. 28, 2005, the objection to claims 1 and 11 has been withdrawn.

26. In view of Applicant's Terminal Disclaimer, filed Sept. 28, 2005, the provisional rejection of claims 1, 5-11, and 15-20 under the under the judicially created doctrine of obviousness-type double patenting as being unpatentable over of copending Application No. 10/692,612 ("Lee I"), in view of Costrini, in further view of Chen, has been withdrawn.

27. In view of Applicant's Terminal Disclaimer, filed Sept. 28, 2005, the provisional rejection of claims 2-4 and 12-14 under the under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over Lee I, in view of Costrini, in further view of Chen, in further view of Wolf I, has been withdrawn.

28. In view of Applicant's Terminal Disclaimer, filed Sept. 28, 2005, the provisional rejection of claims 1, 5, 7-11, 15, and 17-20 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over copending Application No. 10/693,288, ("Lee II"), in view of Chen, has been withdrawn.

29. In view of Applicant's Terminal Disclaimer, filed Sept. 28, 2005, the provisional rejection of claims 6 and 16 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Lee II, in view Chen, in further view of Costrini, has been withdrawn.

30. In view of Applicant's Terminal Disclaimer, filed Sept. 28, 2005, the provisional rejection of claims 2-4 and 12-14 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Lee II, in view of Wolf I, in further view of Chen.

31. Applicant's arguments (Applicant's Remarks, page 15, Section iii. (g)), filed Sept. 28, 2005, regarding the rejection of claims 1, 5-9, 11, and 15-19 under 35 U.S.C. 102(e)/103(a) as being anticipated by or, in the alternative, obvious over Costrini have been fully considered but they are not persuasive.

32. Applicant argues that Costrini does not explicitly or inherently disclose "a single layer of a first mask layer on the etch stop layer" and that Costrini teaches away from a single layer by disclosing that mandrel (60) as comprising of several layer of material (Applicant's Remarks, page 15, Section iii. (g)). However, the Costrini reference does

not support this argument. First, Costrini discloses that, "[t]his feature [the mandrel] is not required, however, for the sidewall spacer formation and a more traditional approach using a conductive hardmask, such as TiN or TaN, can also be used" (paragraph 0013). Second, after disclosing the multilayered mandrel (60), Costrini teaches that, "[a]lternative hardmask materials, such as TiN or TaN, may similarly be used in the patterning process..." (paragraph 0017). In other words, Costrini discloses that either a TiN or TaN hardmask (i.e., a single layer) can be used in place of the mandrel (60) (paragraphs 0013, 0017). Therefore, Applicant's claims 1 and 11 stand anticipated by, or in the alternative, obvious over the Costrini reference.

33. Applicant's arguments (Applicant's Remarks, page 16, Section iii. (h)), filed Sept. 28, 2005, regarding the rejection of claims 2-4 and 12-14 under 35 U.S.C. 103(a) as unpatentable over Costrini, in view of Wolf I, have been fully considered but they are not persuasive, as discussed above.

34. Applicant's arguments (Applicant's Remarks, page 16, Section iii. (i)), filed Sept. 28, 2005, regarding the rejection of claims 10 and 20 under 35 U.S.C. 103(a) as being unpatentable over Costrini, in view of Chen, have been fully considered but they are not persuasive, as discussed above.

Conclusion

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC

EBC
Nov. 1, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER